

## Introduction

In order to meet requirements on a wide flexibility concerning pad geometry and shape of the total pad area covered by ~2000 electronics channels, we here outline a system, based on the ALTRO-chip, which offers the highest level of modularity.

The basic module is a mini-front-end card (mini-FEC) with 32 channels, where each channel corresponds to a pad area of about 4 mm<sup>2</sup>. Thus, it is adopted for pads of size 1x4 mm<sup>2</sup> or bigger and the total pad area can be extended beyond the 2000 channels without getting space problems for the electronics. An alternative solution also described below is the midi-FEC which contains 64 channels. These boards can be connected either directly onto the pad plane or via short cables.

## Connecting readout electronics to a GEM pad-plane

The connector for 32 channels to be mounted on the back of the pad-plane should be a high-density connector smaller than 16x8 mm<sup>2</sup> in order to fit on the area given by a 1x4 mm<sup>2</sup> pad.

An example of such a connector is Japan Aviation Electronics ([www.jae.co.jp](http://www.jae.co.jp)) [WR series](#) connector. This connector offers a 0.5mm pitch and a 40pin connector is 11.5x5 mm<sup>2</sup>.

A 40 pin connector would allow an extra 4 ground-pins per 16 inputs which is a reasonable number of ground connections.

The connector receptacles are offered in both straight and right angle connectors, making them a good choice for vertical plug-in modules.

The choice for a connector mounted on the back of the pad-plane would be the [WR-40S-VFH05-1](#) and the connector to mount vertically of a mini-FEC connected directly at the back of the pad-plane would be [WR-40P-HF-HD](#).

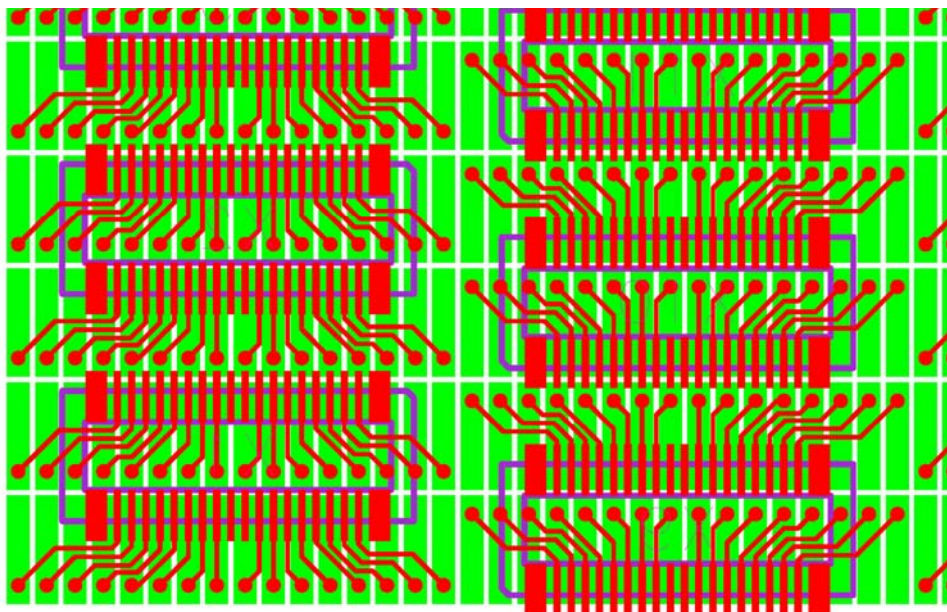


Figure 1) Example of signal routing from 1x4 mm<sup>2</sup> pad to WR-40S (ground routing not shown)

## The mini-FEC

In order to fit a mini-FEC directly on the backside of the pad-plane there are a number of limitations to consider.

The digitization should use the ALTRO chip since this is specially designed for TPC readout. Since the ALTRO processes 16 channels, the modularity of a mini-FEC-card should be a multiple of 16 channels.

The ALTRO chip is only available in a tqfp176 package which has a minimum width of 26 mm edge-to-edge; therefore the minimum width of a mini-FEC should be slightly larger than 26 mm which means it's not enough to read out 16 channels but necessary to readout 32 channels. This means that the module can be minimum 27 mm and maximum 32 mm wide and must contain 2 ALTRO which then can be mounted on each side of the card.

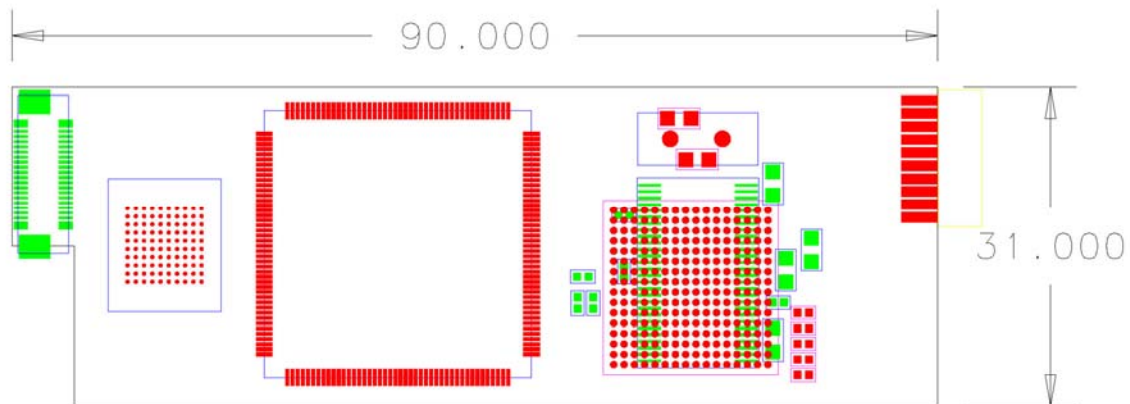
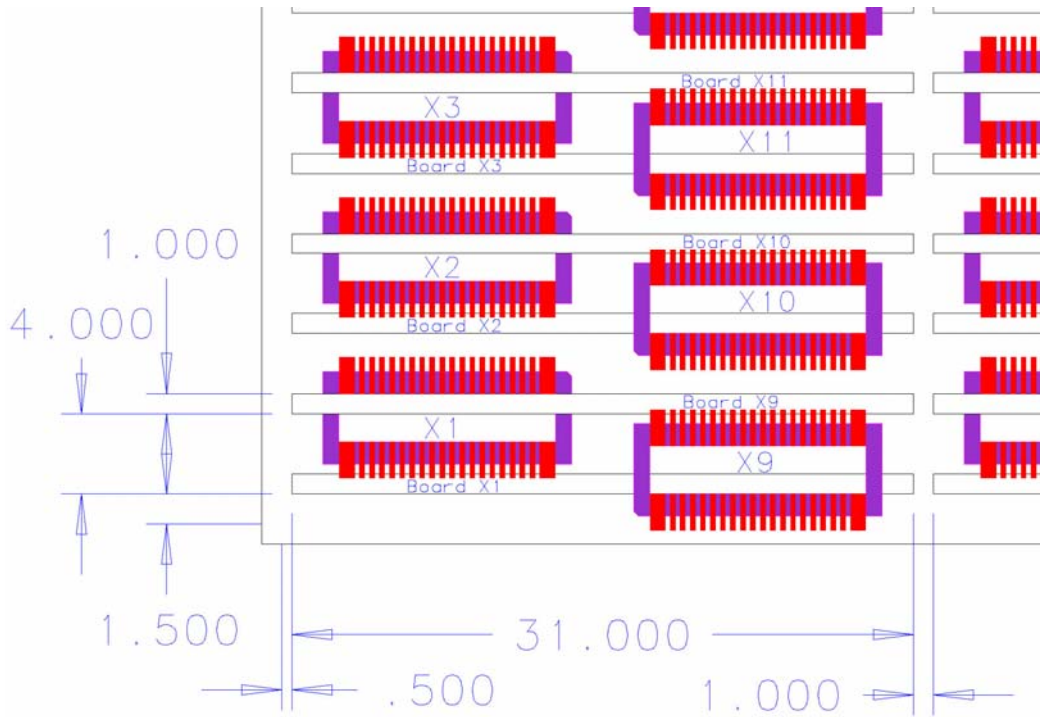


Figure 2) Example of possible layout for single mini-FEC

If the pads are  $1 \times 4 \text{ mm}^2$  pads, the mini-FECs must be placed 4 mm apart.

In order to allow some space for tolerances, the board's maximum width should be 31 mm and the thickness of the PCB itself should be kept to max 1 mm in order to make room for components.

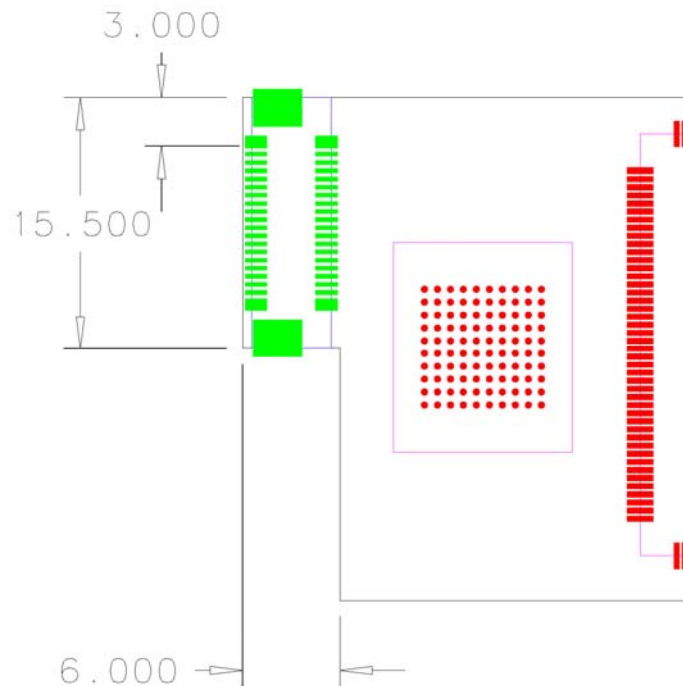


**Figure 3) Size and placement of mini-FECs**

The space between two adjacent boards is 4 mm whereas the width of the connector is 4.7 mm. However, this problem can be solved by making a cut-out in that part of the board that is not occupied by the connector, as illustrated in figure 4. This allows the connector of one board to extend beyond the position of the neighboring board. Thus, the connectors have to be staggered in such a way that every second board has the connector on top and every other's second on bottom.

In figure 3 the arrangement is shown from above, where connector X1 belongs to board X1 and extends beyond board X9, whereas connector X9 is attached to board X9 and extends beyond board X1.

2 connectors must be placed over an array of 32x2 pads in order to give the necessary width of the mini-FEC. Therefore the mini-FEC must have an outline around the connector to allow two boards to be placed together.



**Figure 4) Cutout in mini-FEC to allow neighboring board**

The mini-FEC itself should be capable of handling 32 input channels and it therefore fits two ALTRO chips and two 16-channel amplifiers. There must be some controller-chip handling all settings for the amplifier and ALTRO and it's also necessary to have some buffering of the read-out from the ALTRO.

In order to reduce number of output pins and connectors, it's suggested to include the U2F functionality onto the mini-FEC. In this way there would only be needed one logically large FPGA to do all digital handling of the card thereby reducing the need for multiple FPGAs and buffers.

The suggested layout of figure 2 contains one WR-40P-HF-HD input connector that feeds the inputs of two 16-channel CERN amplifiers (here suggested to be packaged in a [Signetics](#) 10x10 row FBGA with 0.8 mm pitch). The differential outputs from the amplifiers go to two ALTRO chips. The CERNAMPs and ALTROs are depicted to lie directly on the opposite side of the board thereby giving the illusion to be a single chip. The outputs from the ALTROs are processed in an FPGA, suggested here is a Lattice [ispXPLD5768](#) in a 16x16 ball 1mm pitch FBGA package. The FPGA sends and receives data from a CY7C68001 thereby making up a complete U2F card directly mounted on the mini-FEC. The USB signals + power + clock + trigger +... are finally fed to a 20-pin Harwin connector [M50-3001022](#) which is a 1.27mm pin header meant for hole-mounting but which in this case would function as an edge connector.

For voltage regulator needs, the rad-hard [RHFL4913](#) (based on the CERN LHC4913 design) is suggested.

## Dual mini-FEC approach

In order to fit everything more easily within the 4mm spacing, a different approach could be to dock two mini-FECs into a dual mini-FEC.

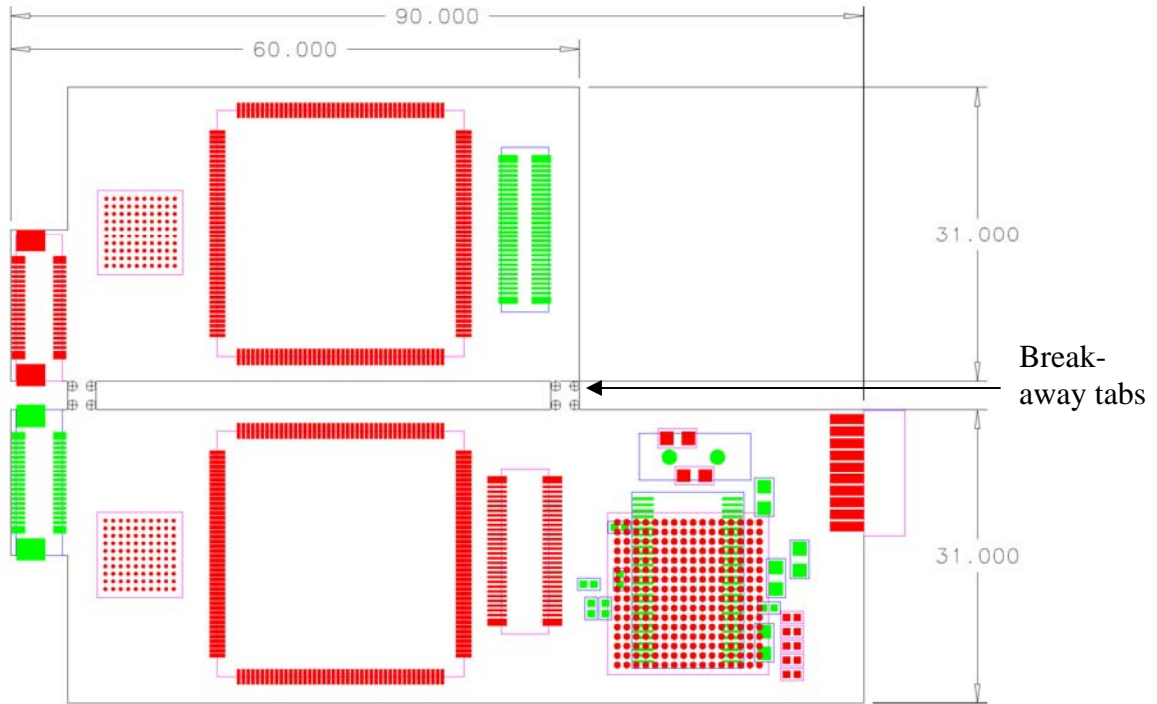


Figure 5) Two mini-FECs to dock to single module

The two boards should be fixed together with some mechanics (screws ...) in order to mount it as a single module.

Such a module should still have a WR-40P connector each for the pair of CERNAMPs on each sub-board in order to equalize input capacitance and noise. However, the outputs from one pair of ALTROs could be collected into a board stacking connector allowing the exact spacing of 3 mm e.g. the [NAIS AXK560145P/AXK660345P](#) pair. The same connectors are also available in a version with 5 mm spacing which would allow the same approach for a  $1 \times 6 \text{ mm}^2$  pad geometry.

This module would utilize only one pair of FPGA + USB-controller thereby reducing overall component count, cost and complexity in the software for only half the number of USB devices.



Figure 6) Docked dual mini-FEC seen from side



Figure 6 gives an idea of how a docked dual mini-FEC could look. Note that the height of the [tqfp176](#) is specified to a maximum of 1.6 mm which can be reduced to 1.45 mm by pushing the pins leveled with the body. This means that the two ALTROs facing each other have to be in physical contact. The height of the ssop56 for the USB-controller as well as the height of the fbga256 for the FPGA is also > 1.5 mm meaning that they won't fit in a 3mm envelope for single boards but relies either on the docking approach or an approach where the chips wouldn't be facing any other chips.

## The midi-FEC

An alternative to a dual mini-FEC could be to accommodate the full 64 channels onto a single board, a mini-double front-end card, midi-FEC. Such a board would have to be large enough to contain 4 each of the CERNAMP and the ALTRO.

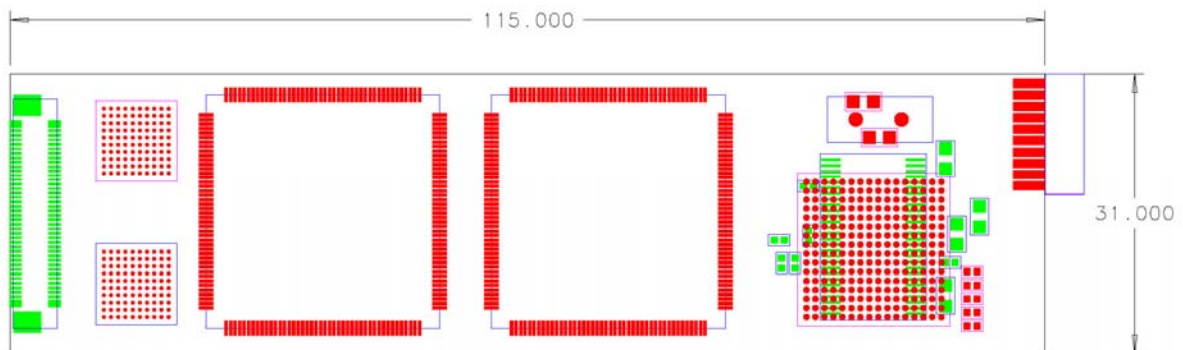


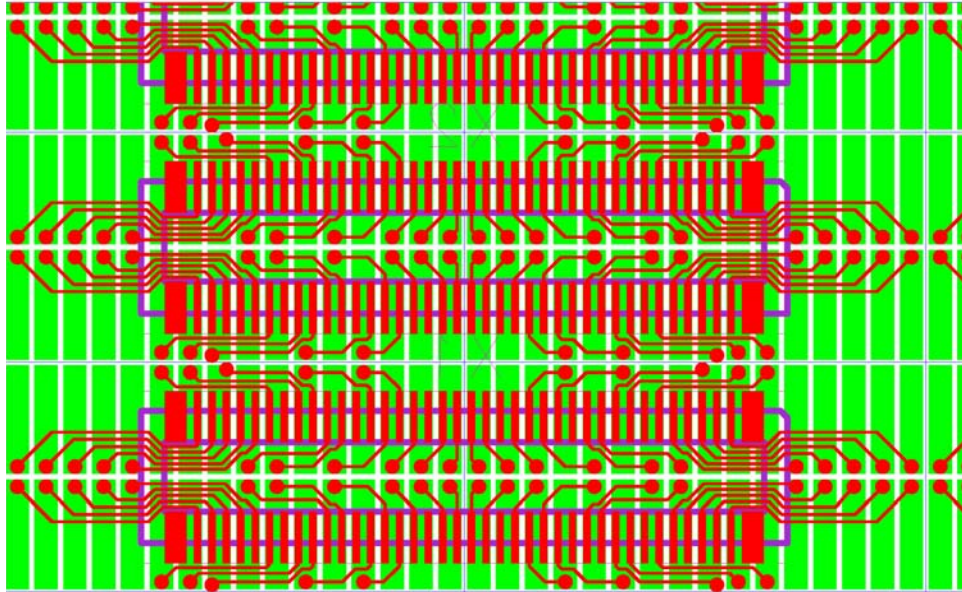
Figure 7) midi-FEC containing 64-channels/4 readout chips

A 64-channel board would mechanically benefit from its increased density by having a single 80-pin WR-80 connector connecting to the pad-plane and by being placed 8mm apart giving ample room for cooling and mechanics.

From an electrical point-of-view however, the board would have to have much higher signal-density and more layers since the signals from 32 channels would have to be passed below one pair of ALTROs to reach the second pair.

There is also an uncertainty about the packaging for the CERNAMPs; a larger package would mean that they too must be placed along the board instead of side-by-side and this would further deteriorate the electrical performance of the board and increase overall length.

The signal routing from pad to connector would look something like figure 8



**Figure 8) pad-routing for a wr-80 connector (ground not routed)**

A further option to all of the above read-out designs would be to add a small intermediate kapton-adapter board. This would allow the front-end electronics to be mechanically disconnected from the pad-plane whilst still retaining same connectors and density.